Agilent Technologies

W-CDMA System Design Simulation and Verification

"Using EDA Connectivity to Test Equipment"

April 30, 2002

presented by:

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Greg Jue

Agenda

- Some of Today's Design Challenges
- Overview of Agilent Technologies Advanced Design System (ADS) and ADS Connected Solutions
- Connected Signal Source Case Study
- Connected Signal Source and Signal Analysis Case Study
- Summary

How familiar are you with W-CDMA?

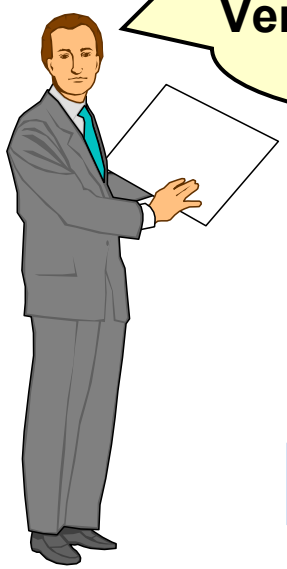
a) I am very familiar with W-CDMA
b) I know the basics of W-CDMA
c) I am not familiar at all with W-CDMA

Design and Verification Challenge:

How Does One Design and Verify to Today's Complex Wireless Formats?

CDMA2000 ?

How do I study today's complex wireless specifications
AND
Partition system requirements
AND
Verify that my design works as parts return from fabrication?



To Do List:

- Study the Wireless Specifications
- Derive Design Requirements from the Specifications
- Verify the RF & System Performance *As Soon As Possible*

3GPP W-CDMA ?

802.11a ?

GSM ?

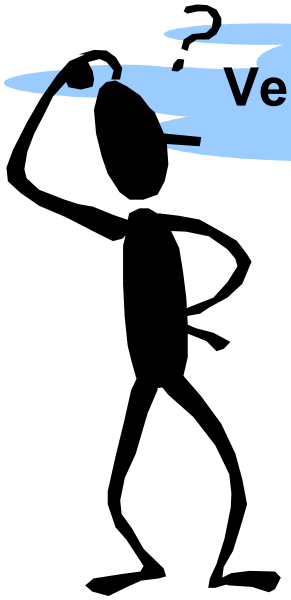
Bluetooth ?

Verification Testing Challenge:

How Does One Begin Testing as Hardware Returns from Fabrication???

Create my own custom test signals, modeling impairments in simulation?

Evaluate re-using existing hardware with a new design modeled in simulation?



Verify hardware as it returns from fabrication before the entire system is built?

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How familiar are you with Agilent's Advanced Design System (ADS) and 3G test equipment?

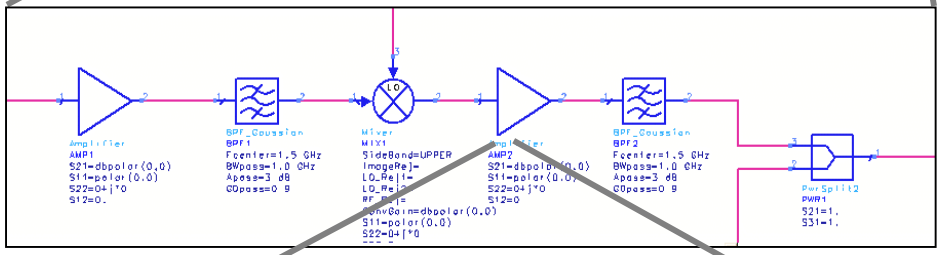
a) Yes, I am familiar with both Agilent's ADS and 3G test equipment
b) I am only familiar with ADS
c) I am only familiar with Agilent's 3G test equipment
d) I am not familiar with either

ADS Top-Down Design Methodology and Bottom-Up Verification:

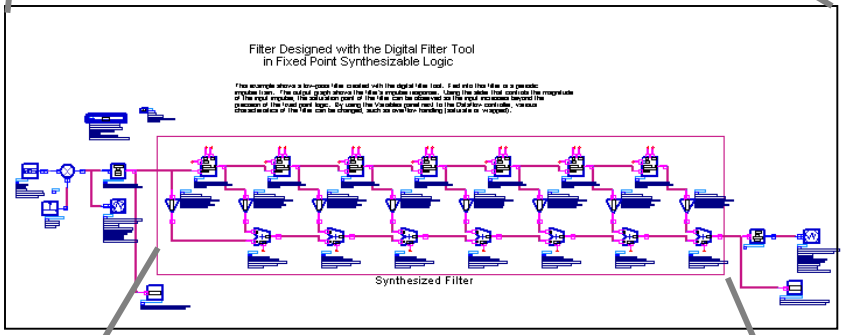
System Level

RF Frontend → RF/Analog Downconverter → Digital Receiver → Demod

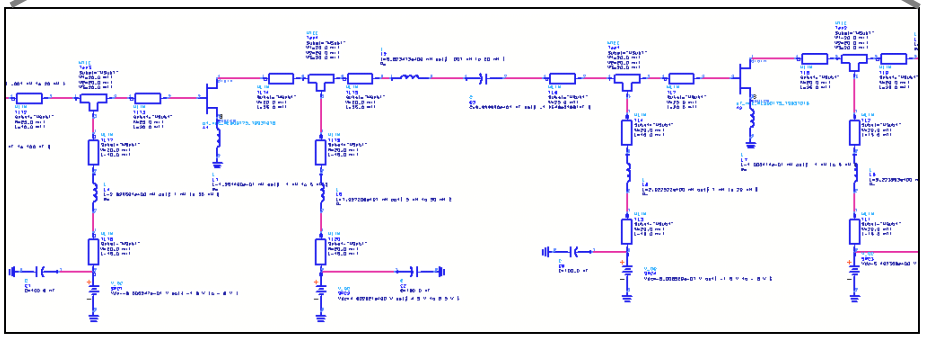
RF/Analog Subsystem



Baseband Floating or Fixed Point



Transistor-level



HDL

```
wire [6:0] M1_B_1_Result;     // hpeesof_id : M1.B_1
wire [9:0] M1_B_2_Result;     // hpeesof_id : M1.B_2

hp_CONST_S C5 (.Result(C5_Result));
defparam C5.Width = 3;
defparam C5.ConstValue = 24576;

hp_ADD_SATTRUNC_S A5
(.A(R4_R1_Q),.B(M3_Result),.Result(A5_Result));
```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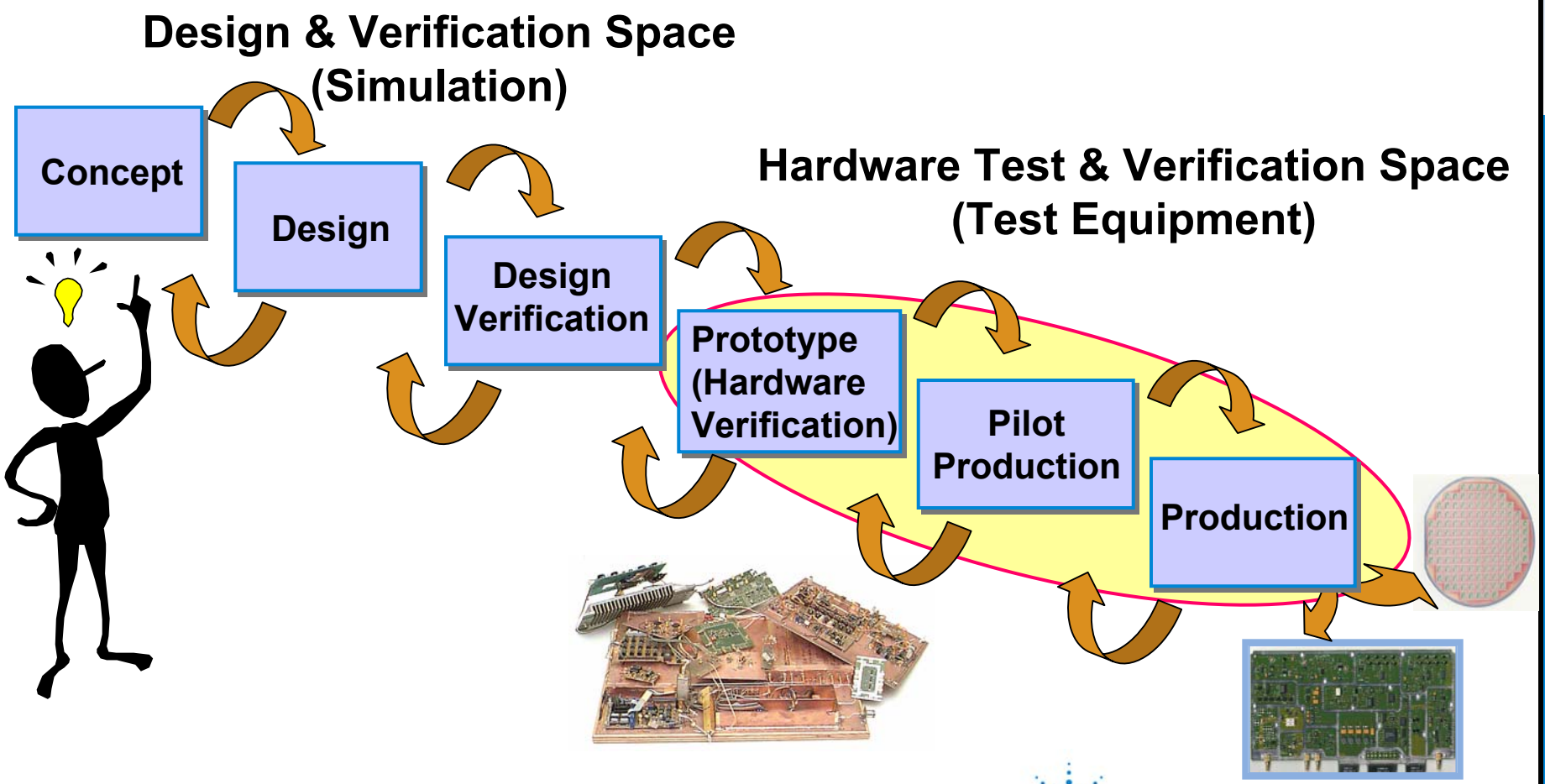
Bridging the Gap Between Design & Test

ADS connected solutions can help bridge the gap between the design & hardware test space



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Connected Signal Source

Creating a Custom Test Signal from Simulation

ESG Sig. Gen. → DUT → 89600 VSA

OR

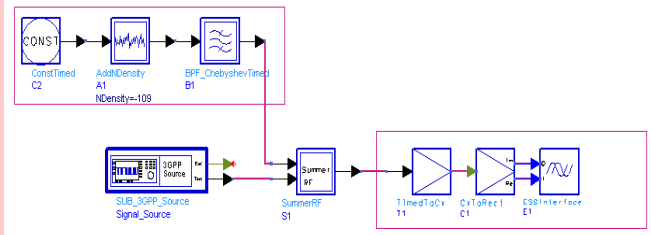
E4440A PSA

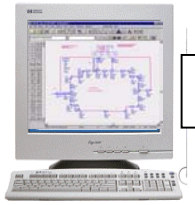
E4406A VSA

ESA-E

Send Simulated Signal to ESG

Modeled Design in ADS





ADS Design SW

Potential applications and benefits include:

- **System Designer**- Create custom test signals with simulation impairments
- **Component Designer**- Use realistic signals for testing
- **Add Impairments**- To evaluate "performance limits"
- **Include Design Distortions**- Model RF circuit / baseband designs in simulaton

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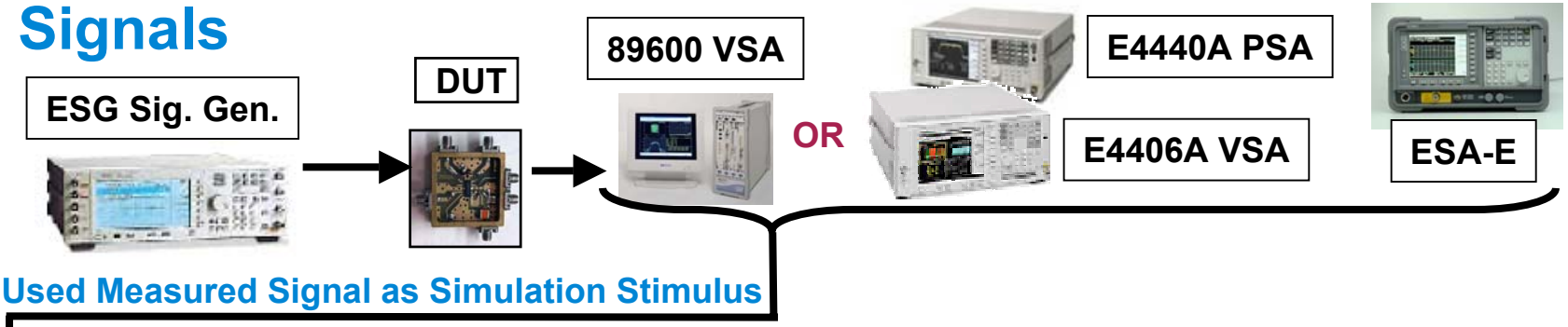
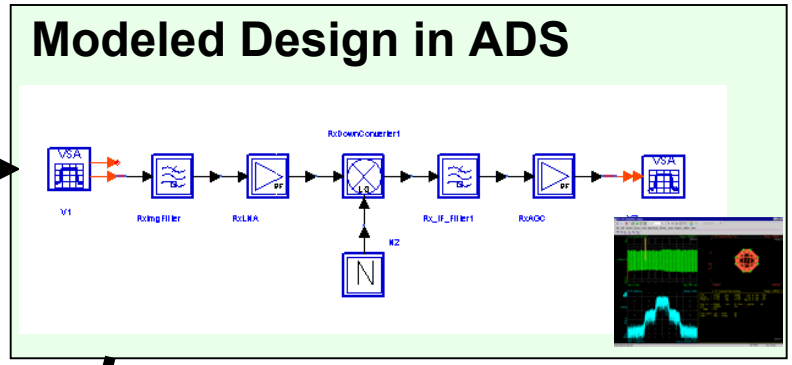
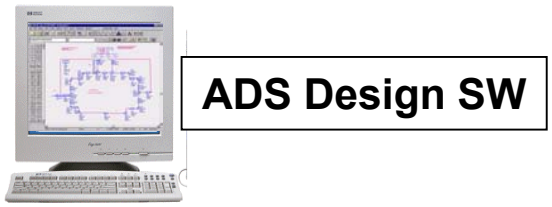
Connected Signal Analysis

Analyzing Your Design in Simulation Using Measured Signals







Potential applications and benefits include:

- **Record Signal on Test Bench**- source the signal into simulation; simulate for verification
- **Model Missing Hardware in Simulation**
- **Reuse Components**- Evaluate off-the-shelf components or existing hardware; simulate impact on system performance

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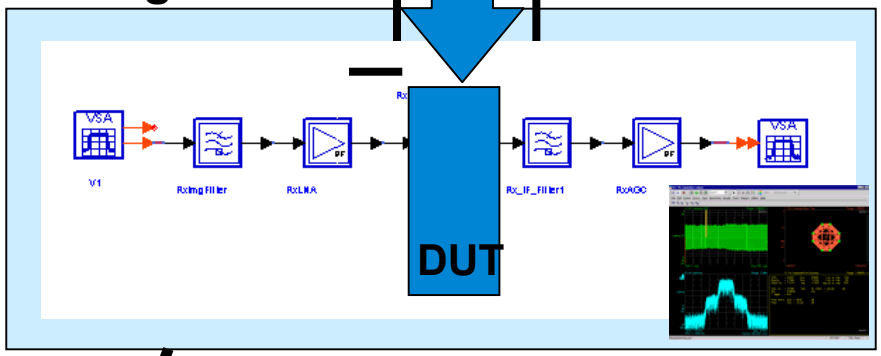
Connected Test Bench

Connected Simulation & Test Solutions

From ADS into ESG

From SA into ADS

Modeled Design in ADS



89600 VSA SW in ADS

ADS Design SW

Potential applications and benefits include:

- **Start End-to-End System Verification** - early using simulation models
- **Replace Simulation Models** - with hardware as it becomes available
- **Identify/ Fix Issues Early** - by verifying performance at every stage
- **Evaluate Reusing Components**

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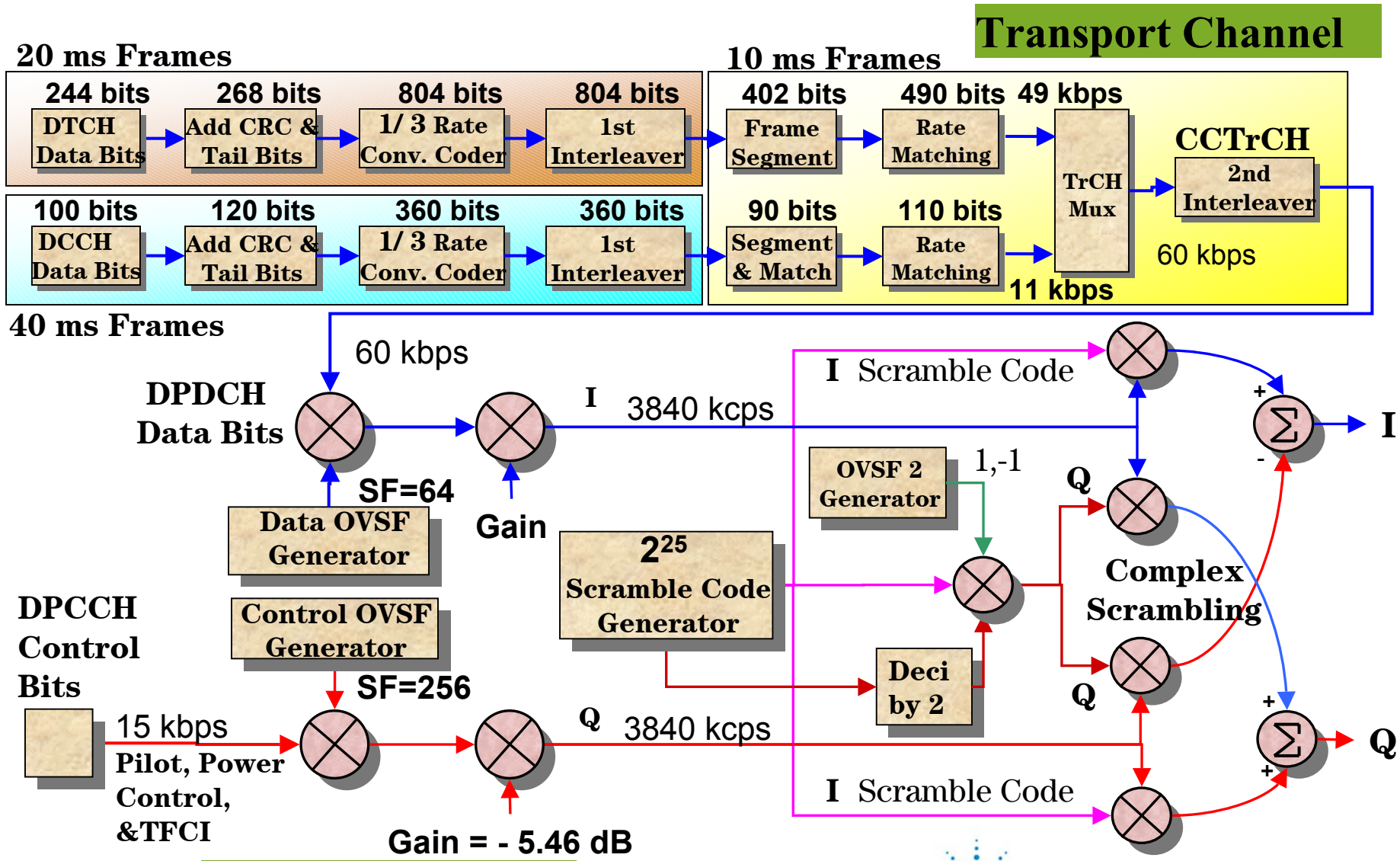
W-CDMA Uplink - RMC 12.2 kbps



Physical Channel

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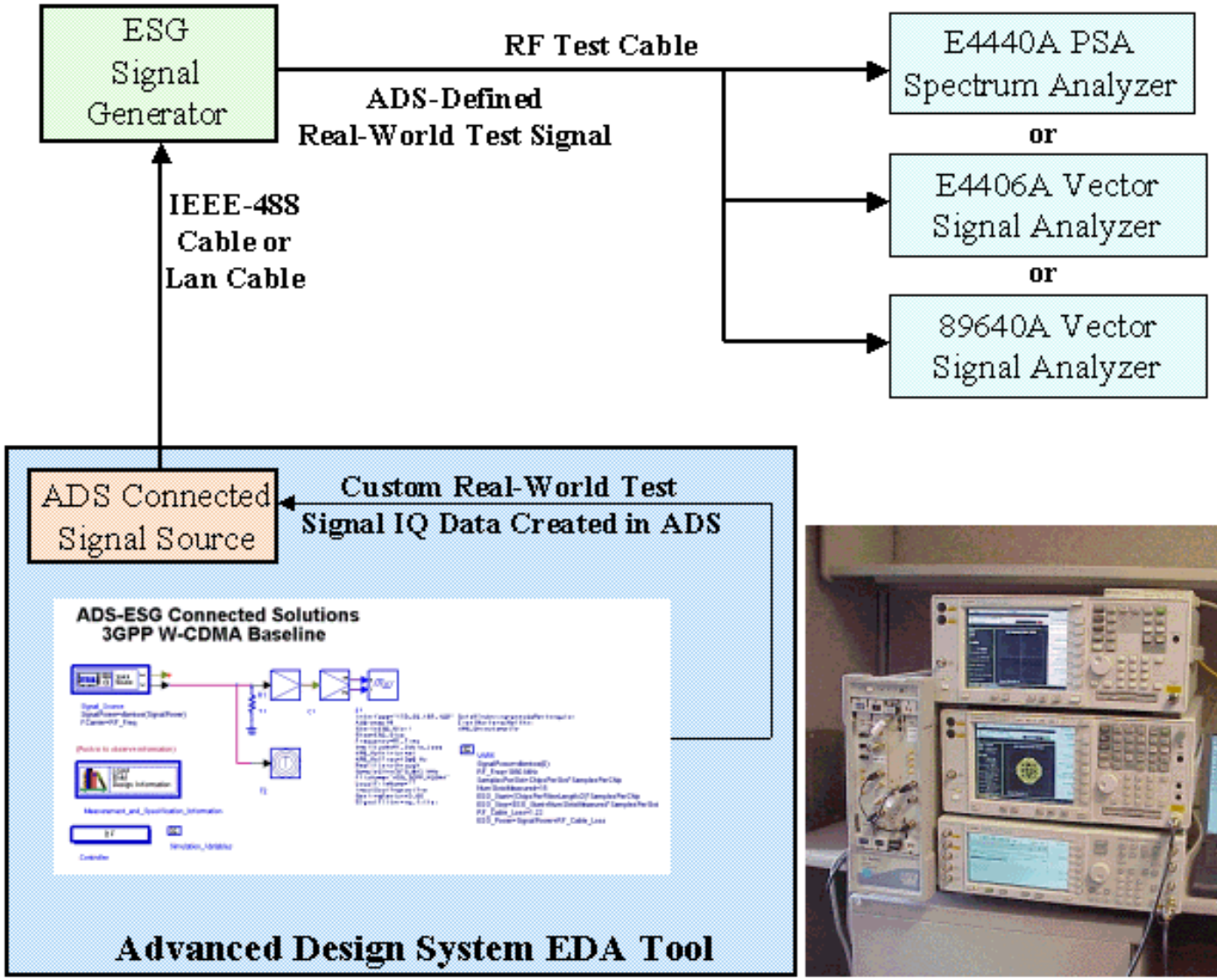
Connected Signal Source Reference Test Setup



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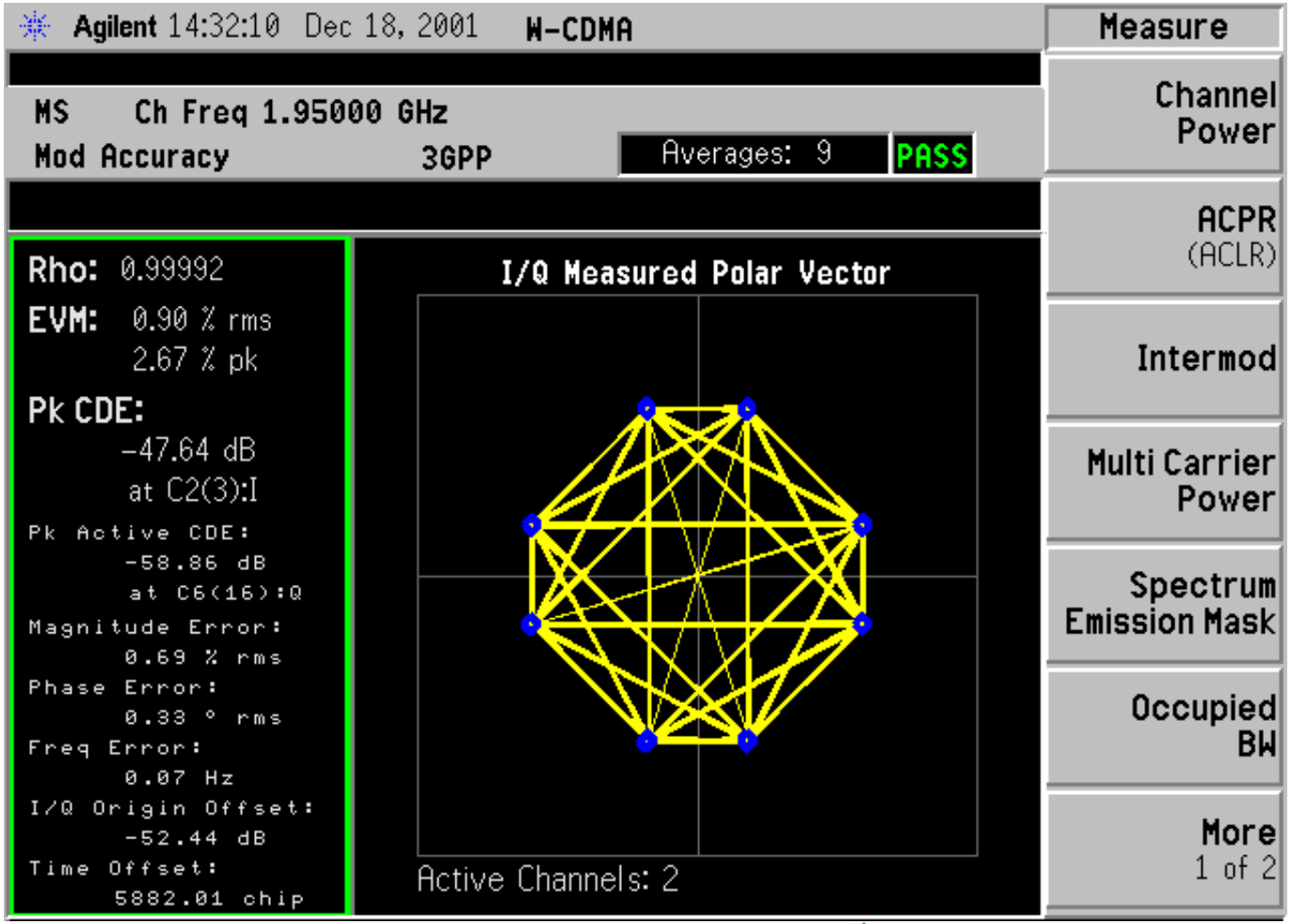
Connected Signal Source Ref. Test Results

ADS-Defined Signal Being Demodulated by Agilent E4440 PSA



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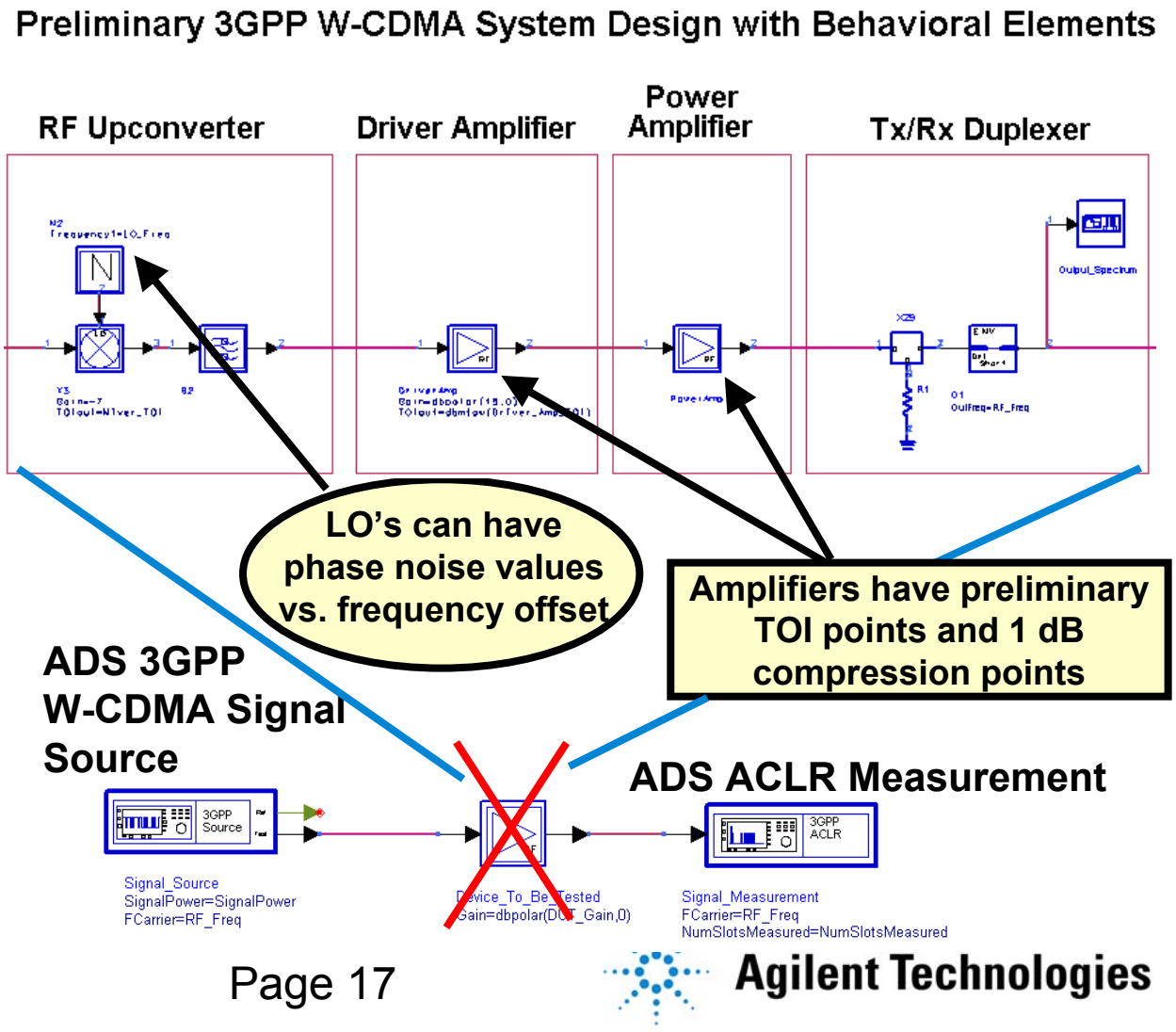
Case Study- Step 1:

Insert Preliminary Top-Level Design into W-CDMA ACLR Pre-Configured Template

- Modify Template for 3G Specification
- Evaluate System Against 3G Spec. ; Partition Requirements
- Design Circuit ; Verify System Performance
- Design Baseband ; Verify System Performance with RF
- Begin Early Verification Testing with Connected Signal Source Solutions



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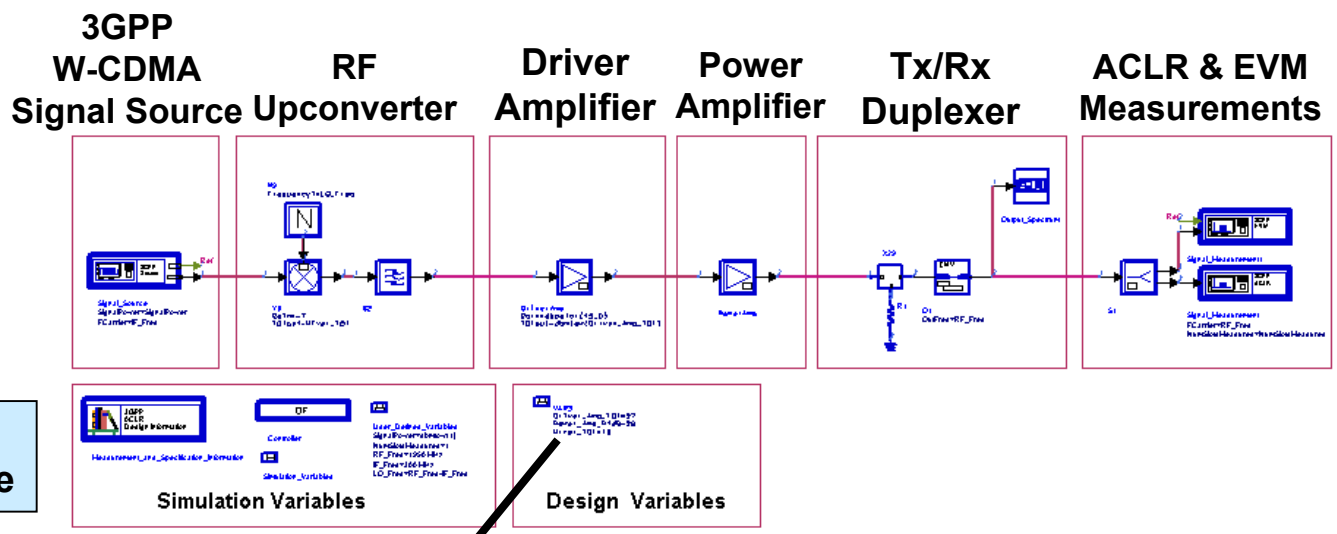
Case Study- Step 2:

Perform System-Level Design Tradeoffs; Partition Circuit Design Requirements

- Modify Template for 3G Specification
- Evaluate System Against 3G Spec. ; Partition Requirements
- Design Circuit ; Verify System Performance
- Design Baseband ; Verify System Performance with RF
- Begin Early Verification Testing with Connected Signal Source Solutions

Preliminary 3GPP W-CDMA System Design with Behavioral Elements



ACLR_U10	ACLR_U5
69.400944	34.920973

Var Eqn

VAR3
Driver_Amp_TOI=27
Power_Amp_P1dB=28
Mixer_TOI=16

Final Circuit Design Requirements

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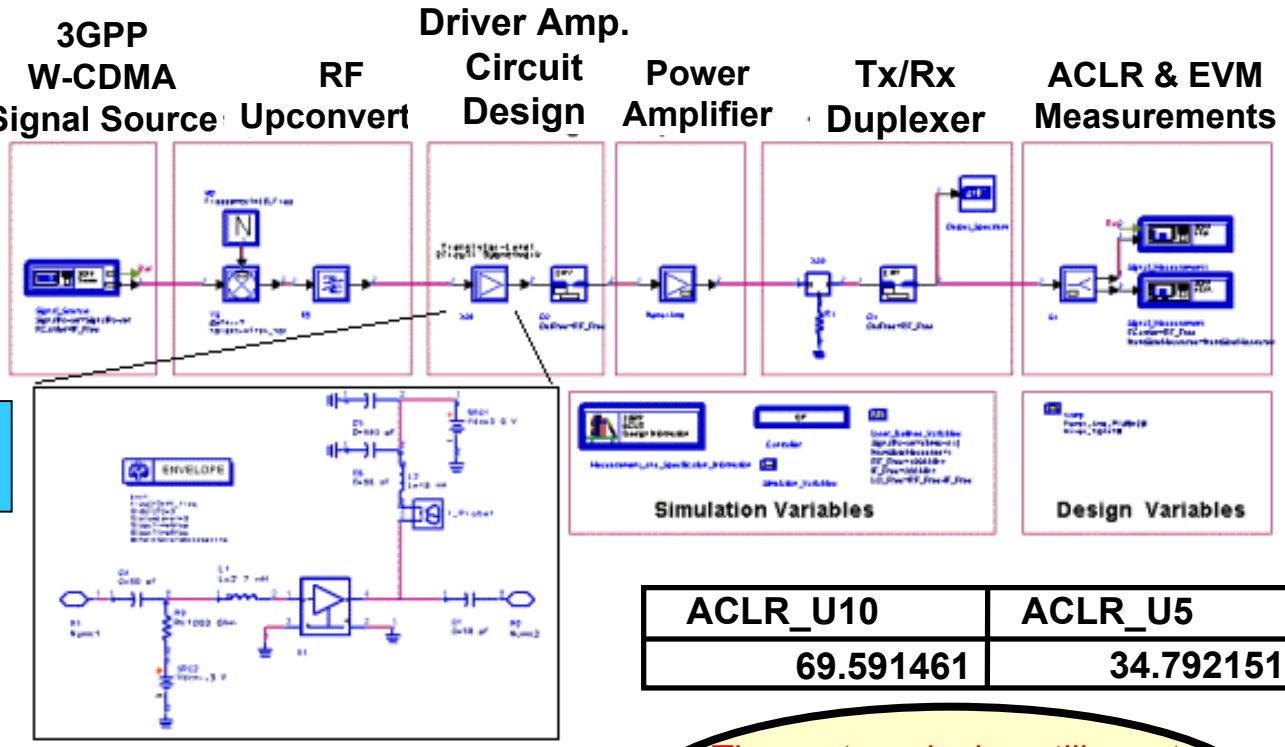
Case Study- Step 3:

Design/Re-Use Circuit; Insert Circuit Design into Top Level System Design for Verification

- Modify Template for 3G Specification
- Evaluate System Against 3G Spec. ; Partition Requirements
- **Design Circuit ; Verify System Performance**
- Design Baseband ; Verify System Performance with RF
- Begin Early Verification Testing with Connected Signal Source Solutions

3GPP W-CDMA System Design Verification with Transistor-Level Circuit Design



Transistor-Level Circuit Design

ACLR_U10	ACLR_U5
69.591461	34.792151

The system design still meets the 3GPP W-CDMA specifications with the detailed circuit design

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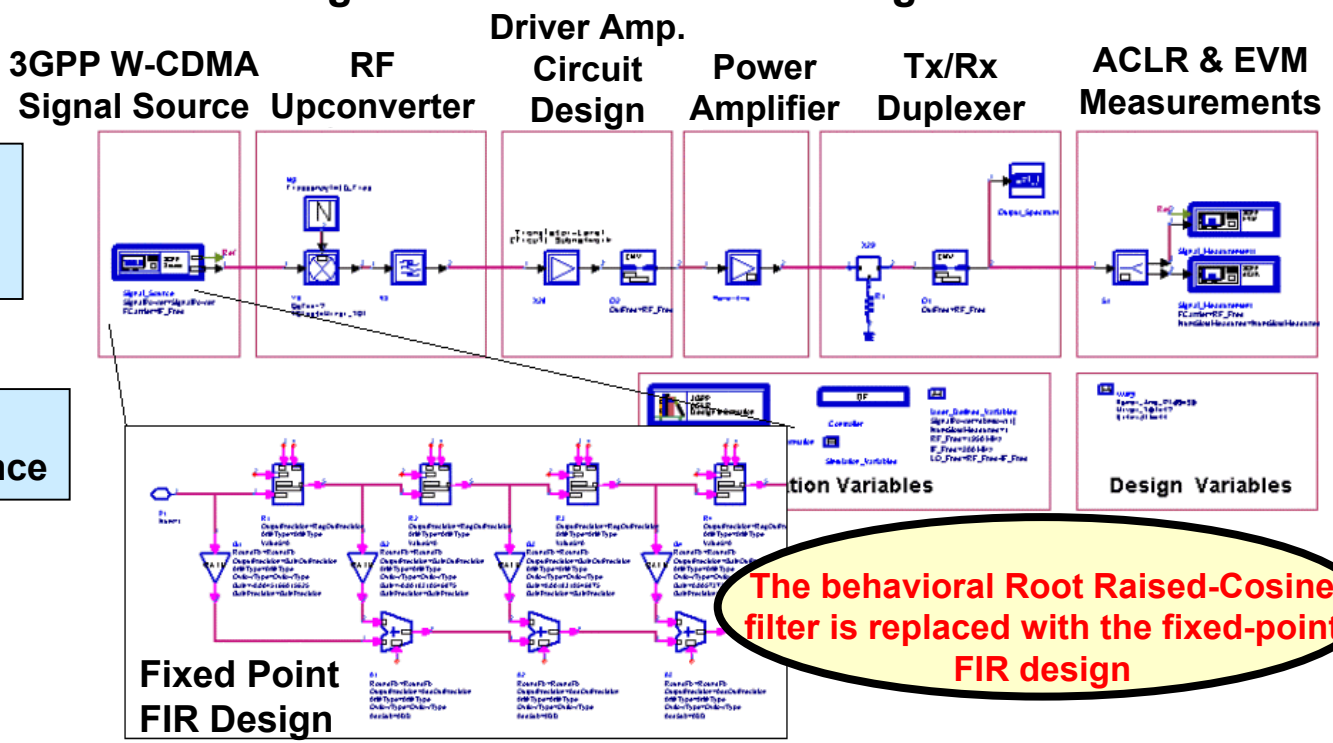
Case Study- Step 4:

Design Baseband; Insert FIR Design into Top Level System Design for Verification

- Modify Template for 3G Specification
- Evaluate System Against 3G Spec. ; Partition Requirements
- Design Circuit ; Verify System Performance
- Design Baseband ; Verify System Performance with RF
- Begin Early Verification Testing with Connected Signal Source Solutions

Final 3GPP W-CDMA System Design with Transistor-Level Circuit Design and Fixed Point FIR Design



The behavioral Root Raised-Cosine filter is replaced with the fixed-point FIR design

The system does not meet specifications of 33 dB @ 5 MHz offset and 43 dB @ 10 MHz offset with baseband and RF designs simulated together...

ACLR_U10	ACLR_U5
37.656388	31.952861

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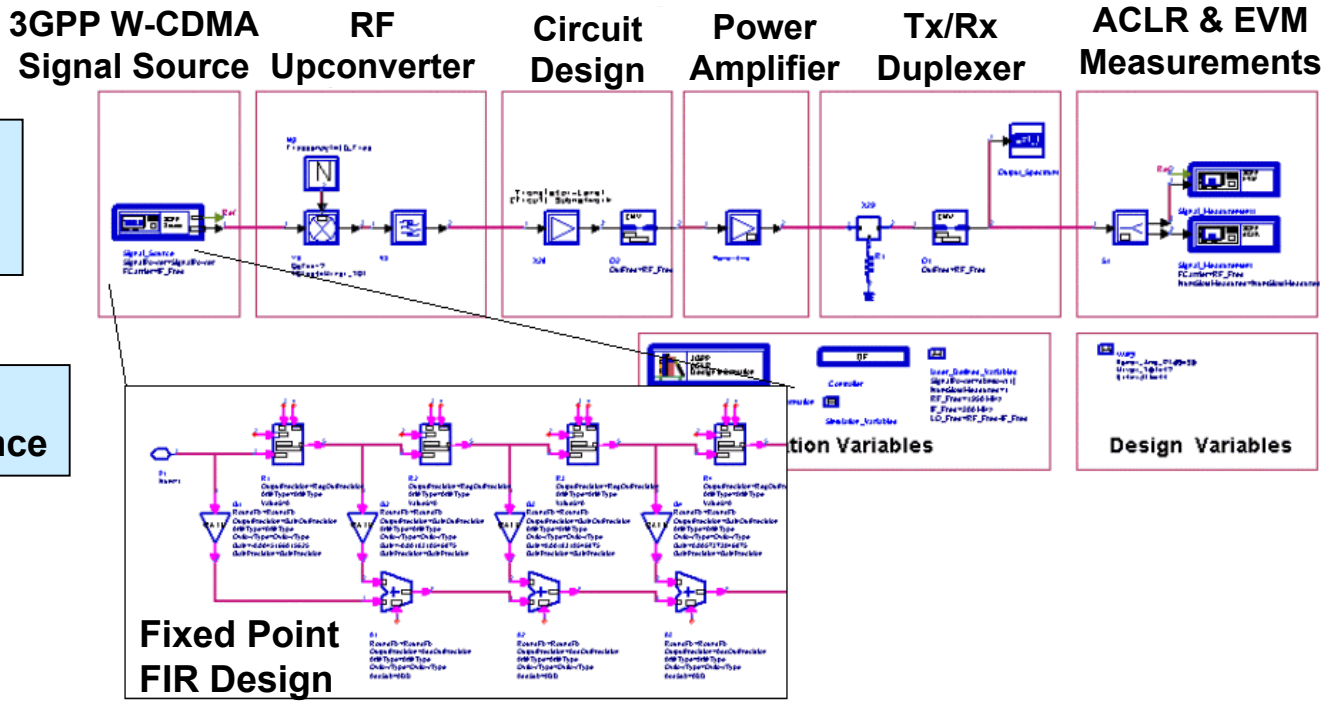
Case Study- Step 5:

Tune/Modify RF and Baseband Designs Together to Meet Specifications

- Modify Template for 3G Specification
- Evaluate System Against 3G Spec. ; Partition Requirements
- Design Circuit ; Verify System Performance
- Design Baseband ; Verify System Performance with RF
- Begin Early Verification Testing with Connected Signal Source Solutions

Final 3GPP W-CDMA System Design with Transistor-Level Circuit Design and Fixed Point FIR Design



The system now meets the 3GPP W-CDMA specification with the baseband design co-simulated with the RF design …potentially saving costly design turns !

ACLR_U10	ACLR_U5
49.201045	34.646249

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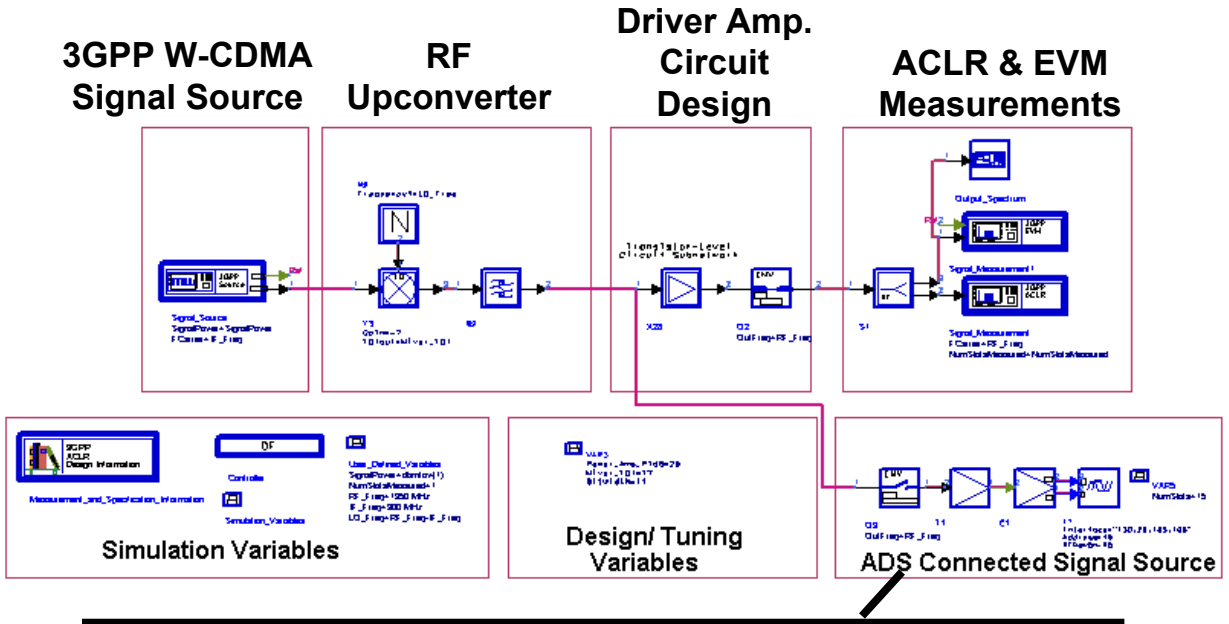
Case Study- Step 6:

Use Connected Signal Source for Early Verification Testing of RF Amplifier

- Modify Template for 3G Specification
- Evaluate System Against 3G Spec. ; Partition Requirements
- Design Circuit ; Verify System Performance
- Design Baseband ; Verify System Performance with RF
- Begin Early Verification Testing with Connected Signal Source Solutions

3GPP W-CDMA Early Design Verification Test using Connected Signal Source Solutions



The output of the ESG contains the RF and fixed point design impairments. This allows the power amplifier prototype to be evaluated **before the entire system is built**

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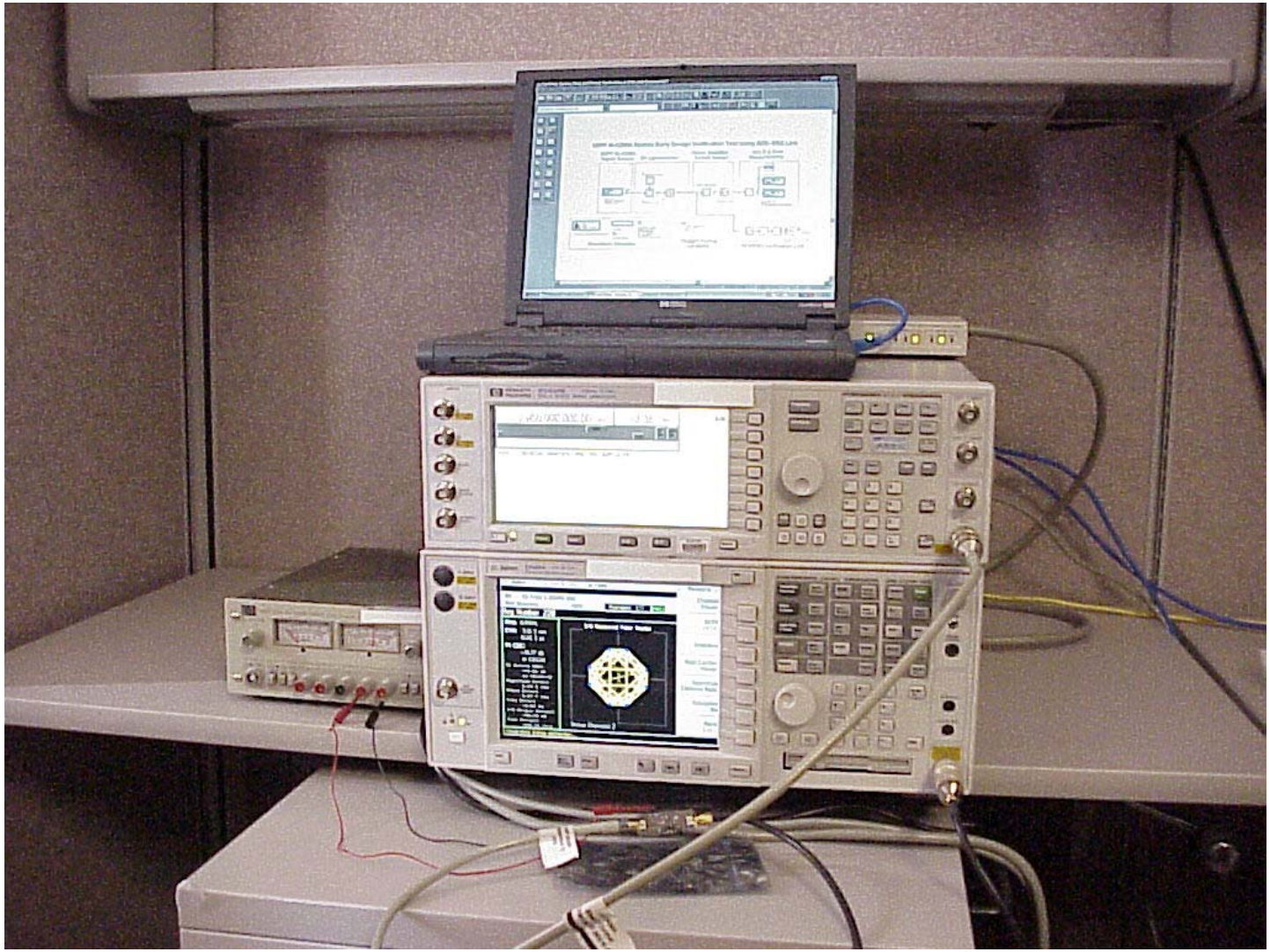
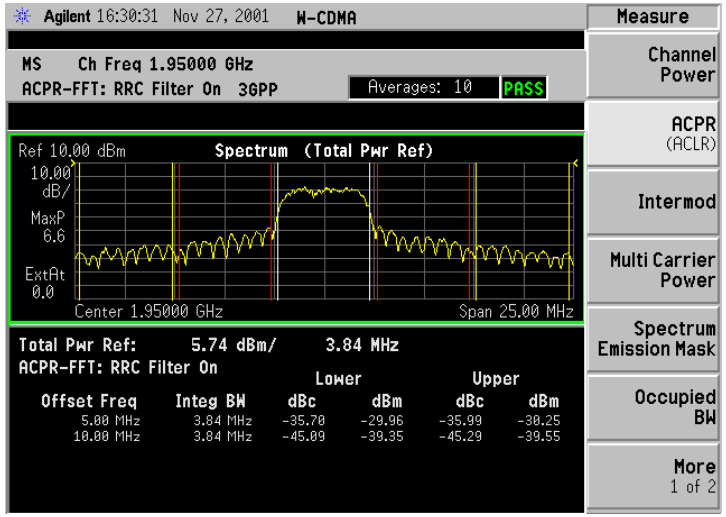
Connected Solutions Test Setup

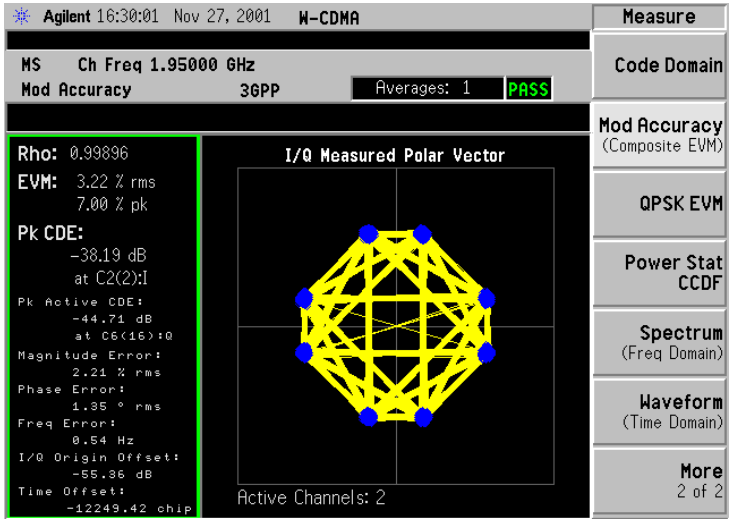


Case Study- Step 7:

Simulated and Measurement Results at Output of the Amplifier D.U.T.



W-CDMA ACLR Meas. - E4440A PSA -



W-CDMA EVM Meas. - E4440A PSA -

The simulated results agree well to measured, especially at the 5 MHz offsets:

Offset	Simulated	Measured
ACLR @ 5 MHz upper offset	35.9 dB	35.9 dB
ACLR @ 5 MHz lower offset	35.9 dB	35.7 dB
ACLR @ 10 MHz upper offset	44.4 dB	45. 3 dB
ACLR @ 10 MHz lower offset	44.1 dB	45.1 dB
EVM	2.98%	3.2%

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Connected Solutions BER

EVM

- Transmitter specification
- Fast and useful for troubleshooting Tx and Rx errors
- Use uncoded signals

BER

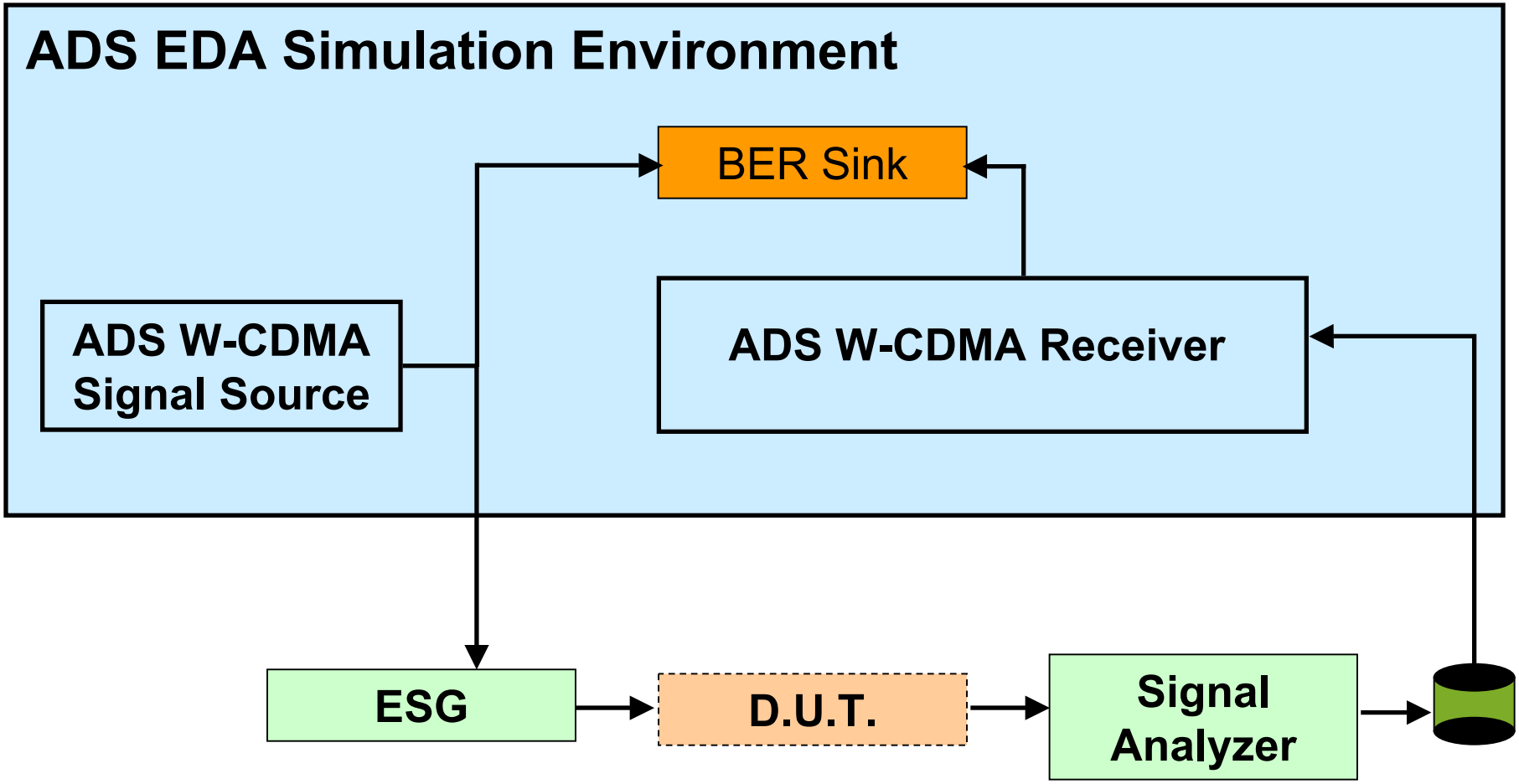
- Receiver specification
- Long simulation times
- Challenging measurement
- Requires coded signals and receiver (RF & baseband)

ADS + ESG + Signal Analyzer Connected Solutions

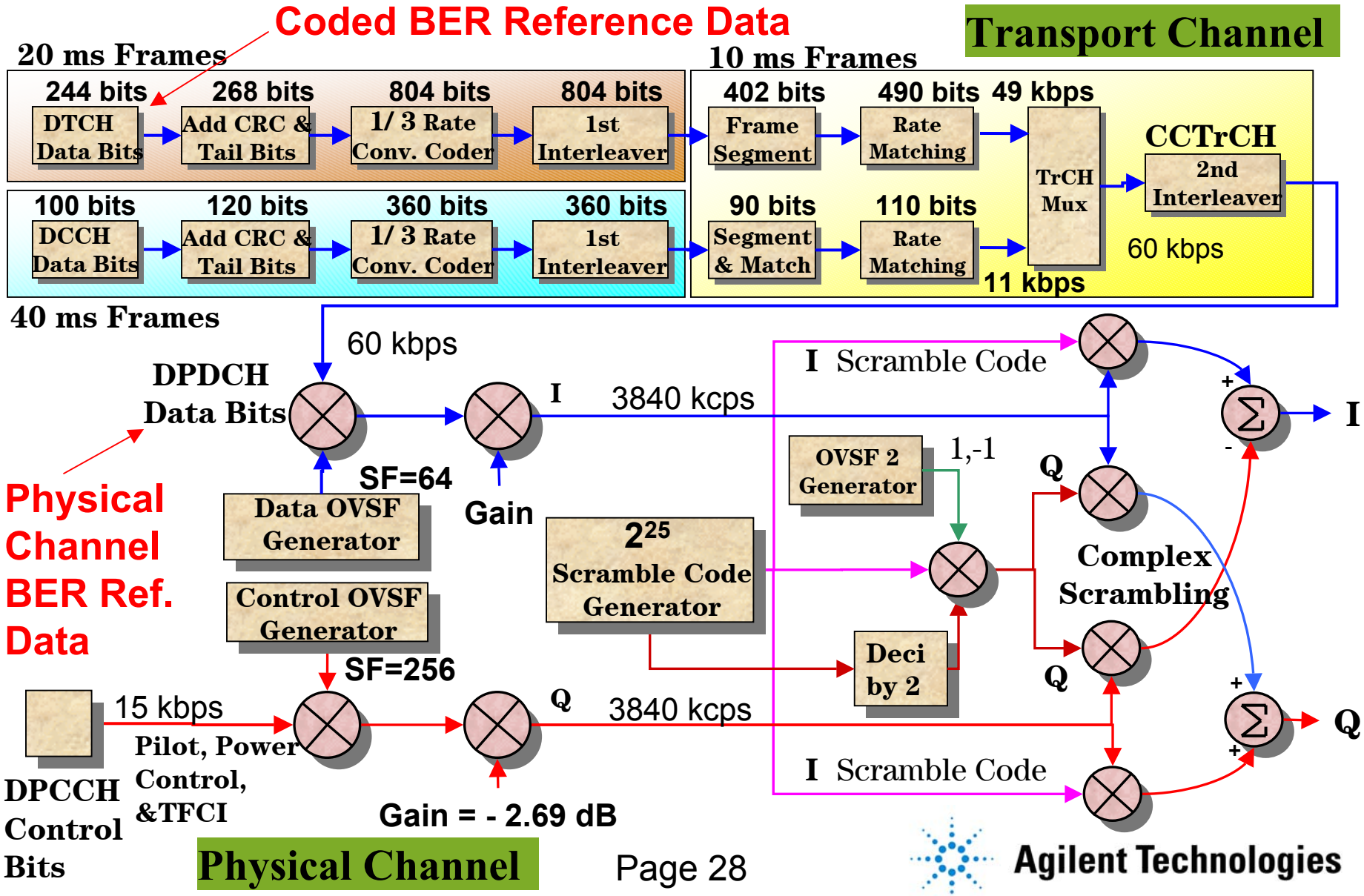
- May offer *early* BER testing of prototype designs
- Can use VSA signal recordings and *ADS-based receiver models*

Case Study:

Conceptual Signal Flow for Connected Solution BER



Coded BER vs. Physical Channel BER



Physical Channel

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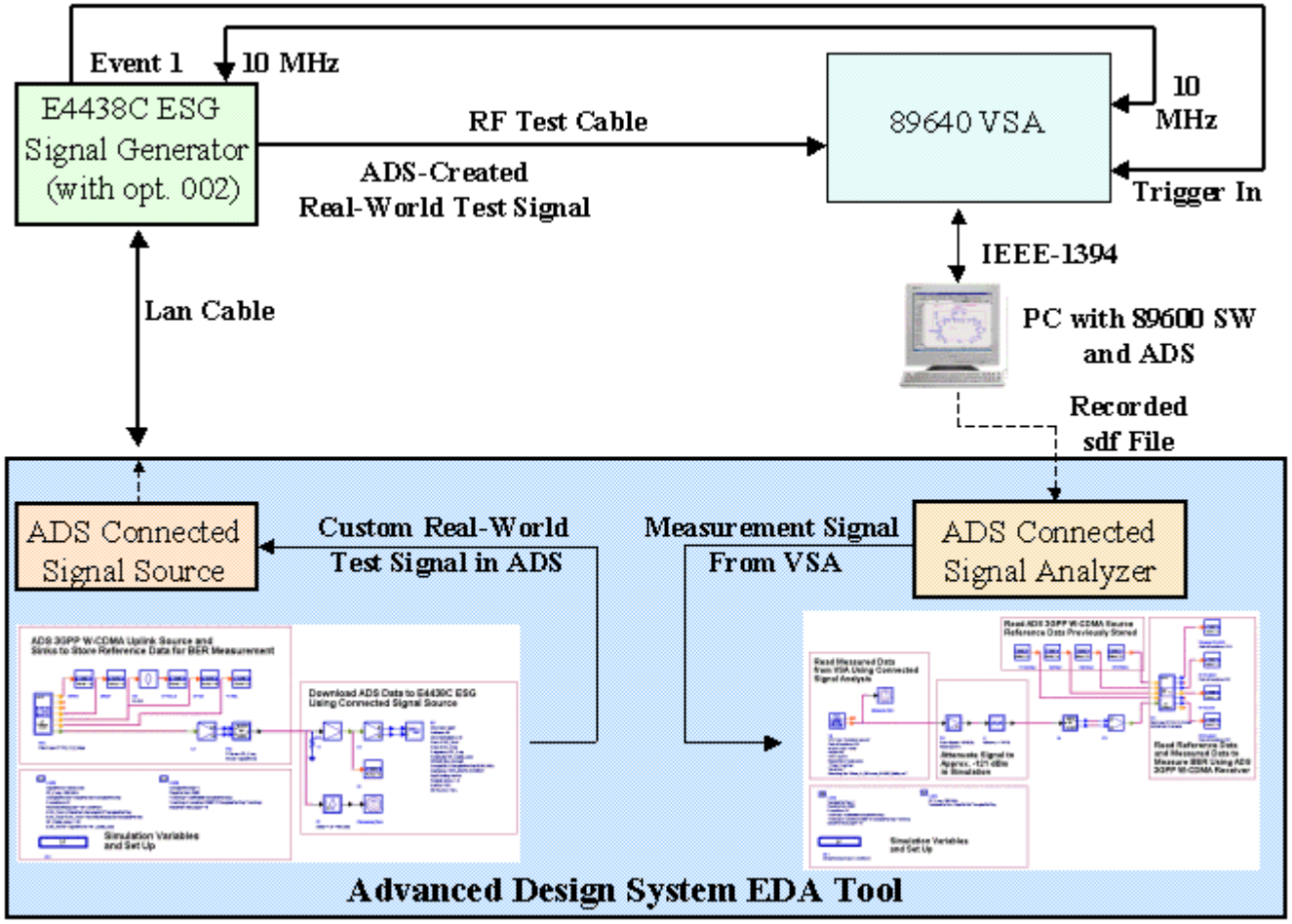
Case Study:

Preliminary Investigation

Test Setup for Connected Solutions BER



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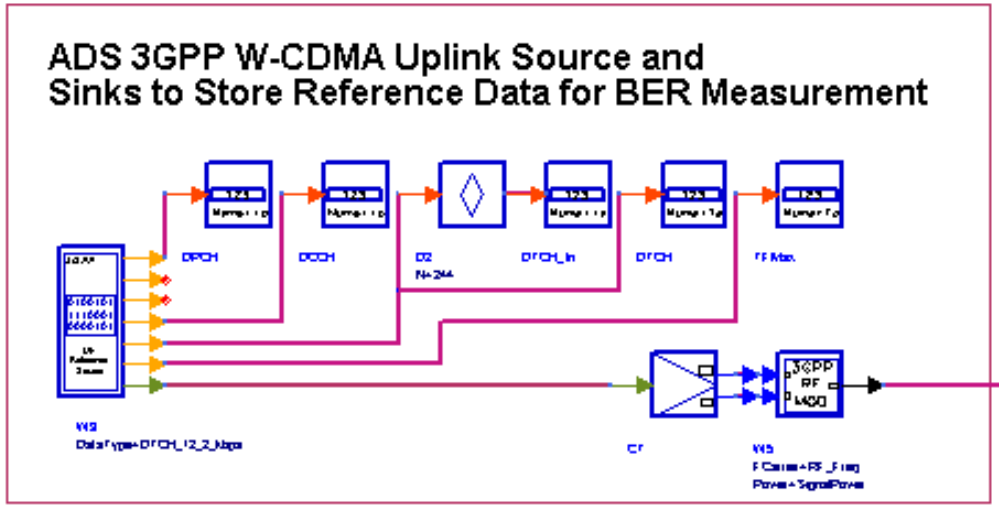
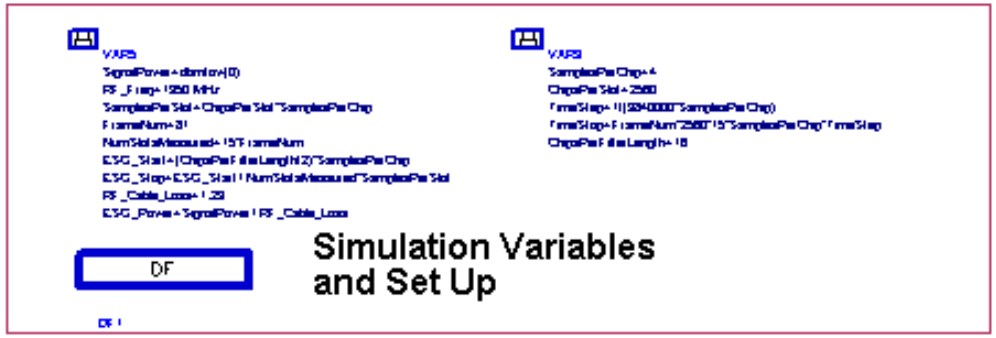
Case Study: Step 1

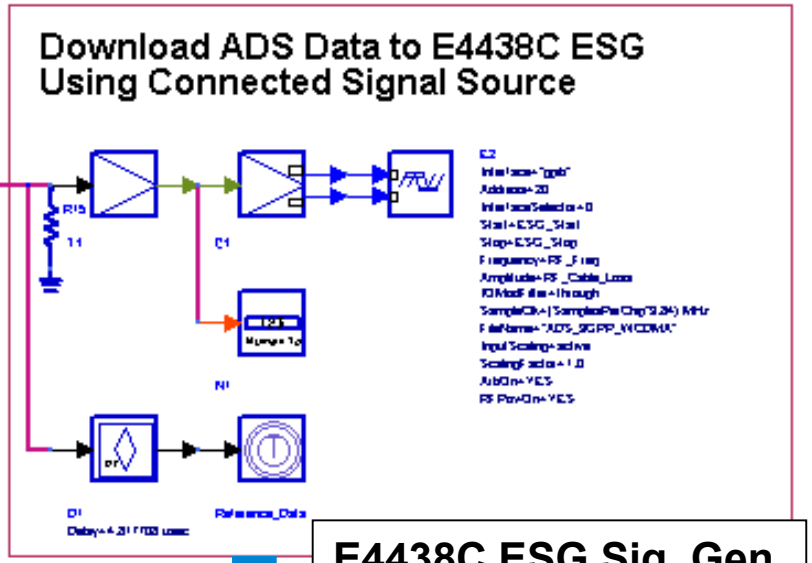
Preliminary Investigation

Run ADS Connected Signal Source Schematic to Turn Simulation Signal into Real RF Test Signal





Download 80 frames of data



E4438C ESG Sig. Gen.

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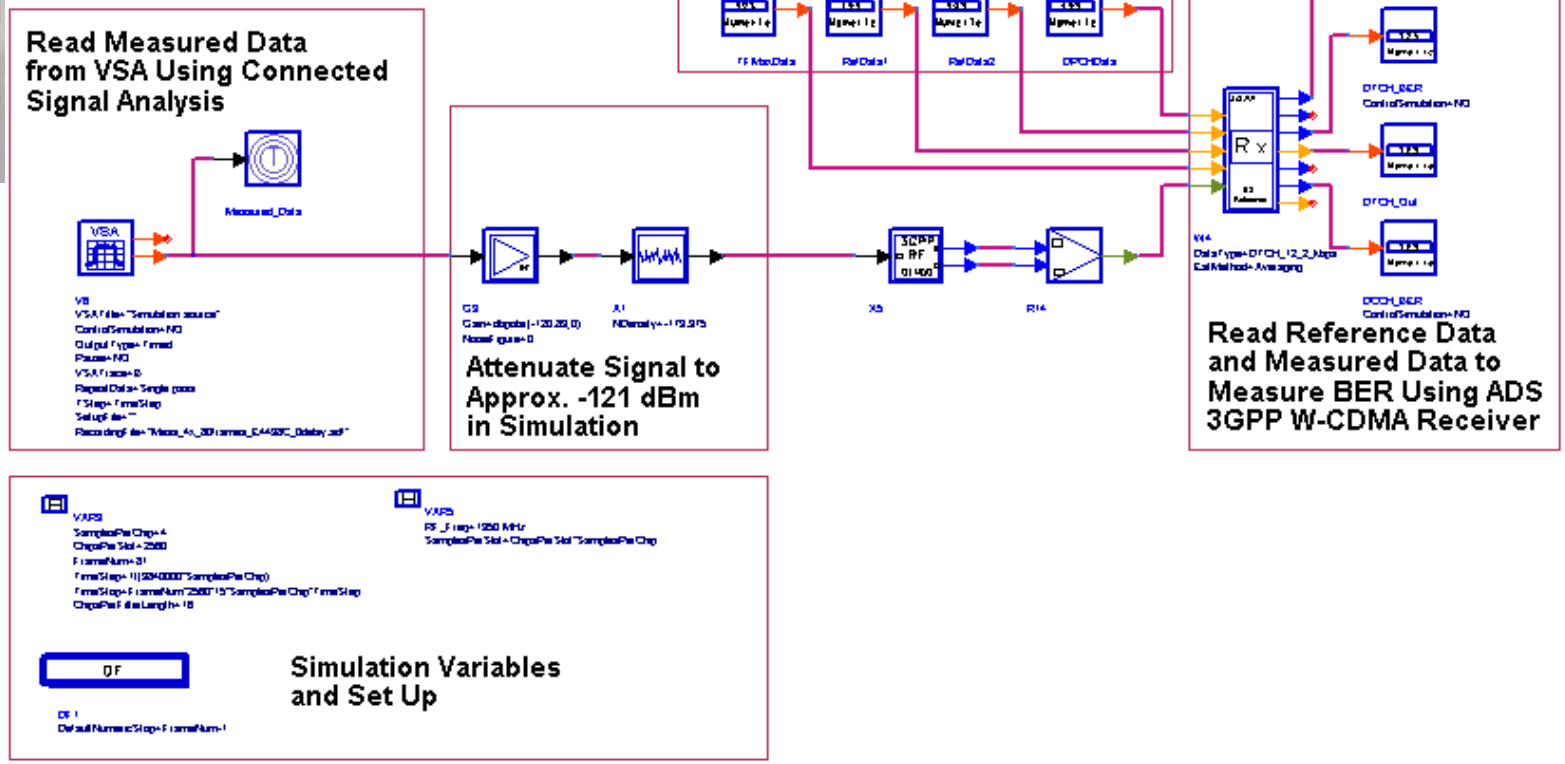
Case Study: Step 2

Preliminary Investigation

Run ADS Connected Signal Analysis Simulation to Perform Connected Solutions Coded BER

89640 VSA

Set Event Triggering on ESG & VSA
Record Waveform
Read Recording into ADS



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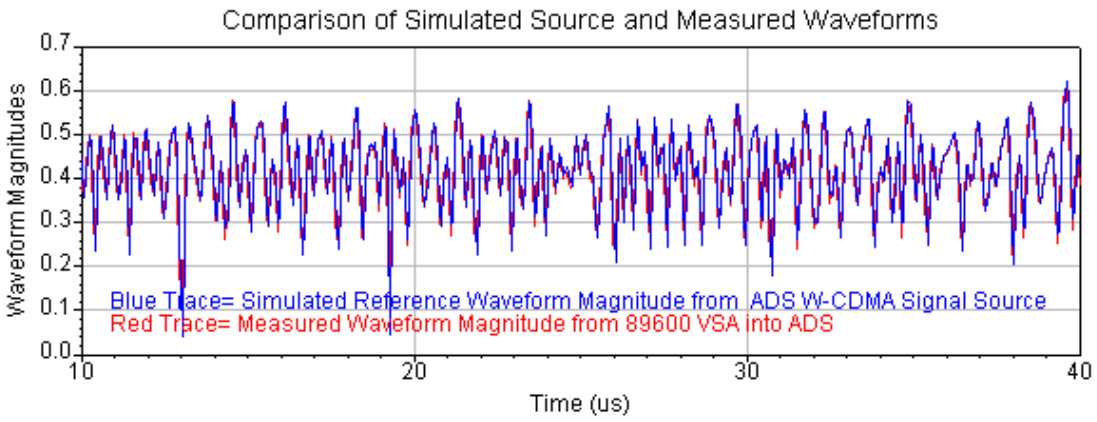
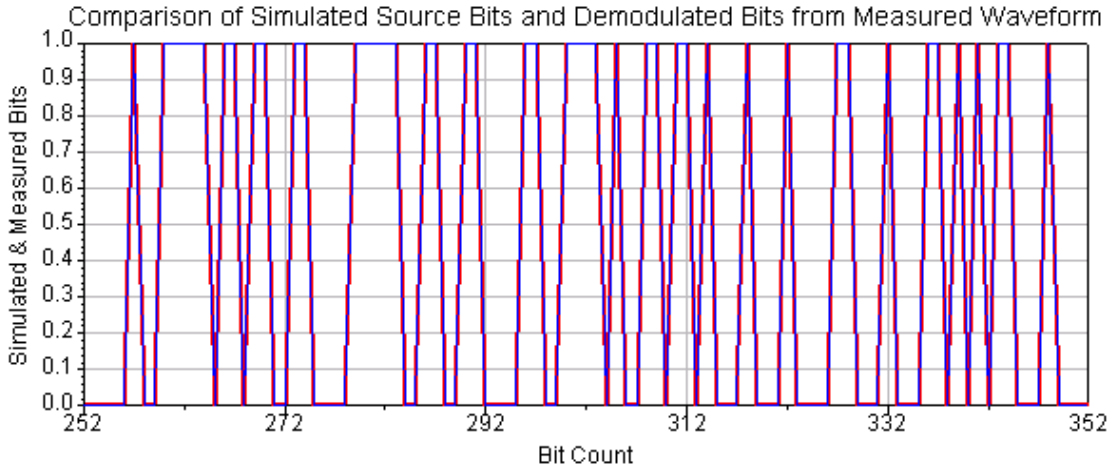
Case Study: Step 3 Preliminary Investigation

View Connected Solutions Waveform and Demodulated Bits (Preliminary Findings)

Waveform Magnitudes



Demodulated Bits



Original ADS Waveform and Measured Waveform Compare Well

Blue Trace= Simulated Signal
Red Trace= Measured Signal

Original ADS Bits and Bits from Demodulating Measured Signal in ADS Compare Well

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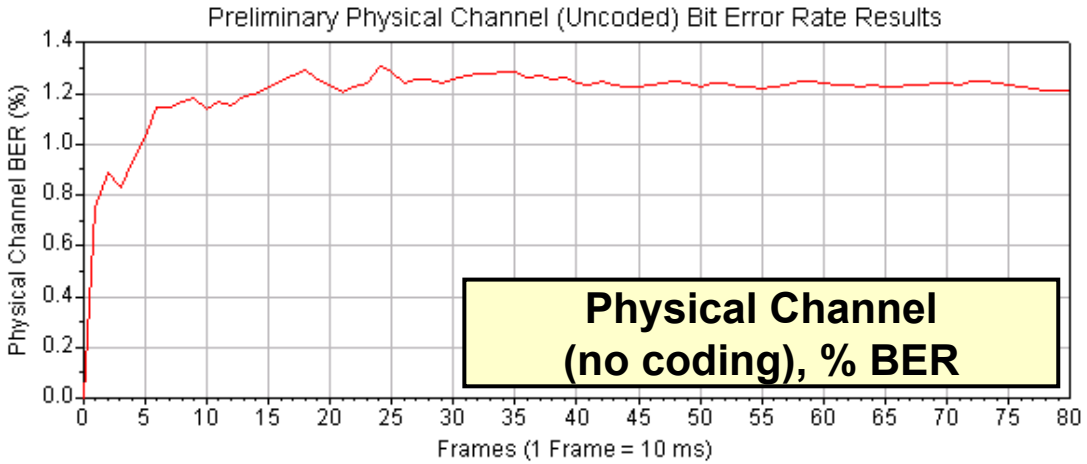
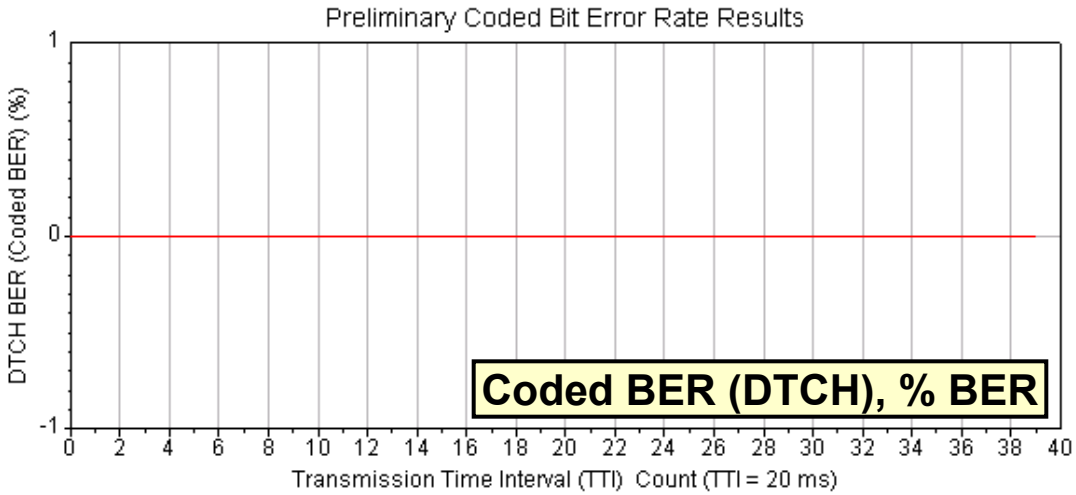
Case Study: Step 4

View Connected Solutions Bit Error Rate Results

(Preliminary Findings)

Preliminary BER Results for Physical Channel and DTCH (% BER)

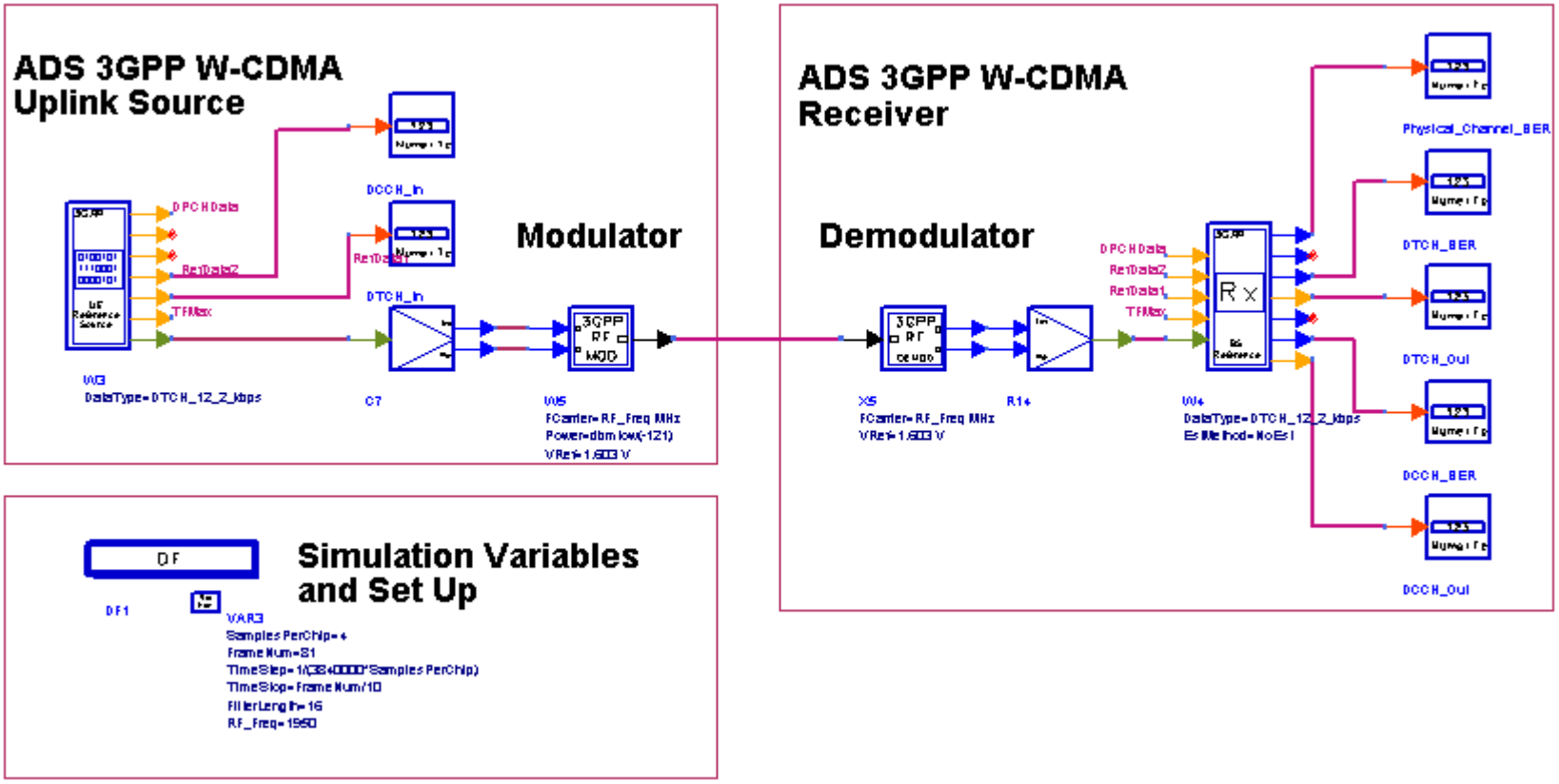




Case Study: Step 5

Preliminary Investigation

Run Simulation-Only BER Simulation for Comparison



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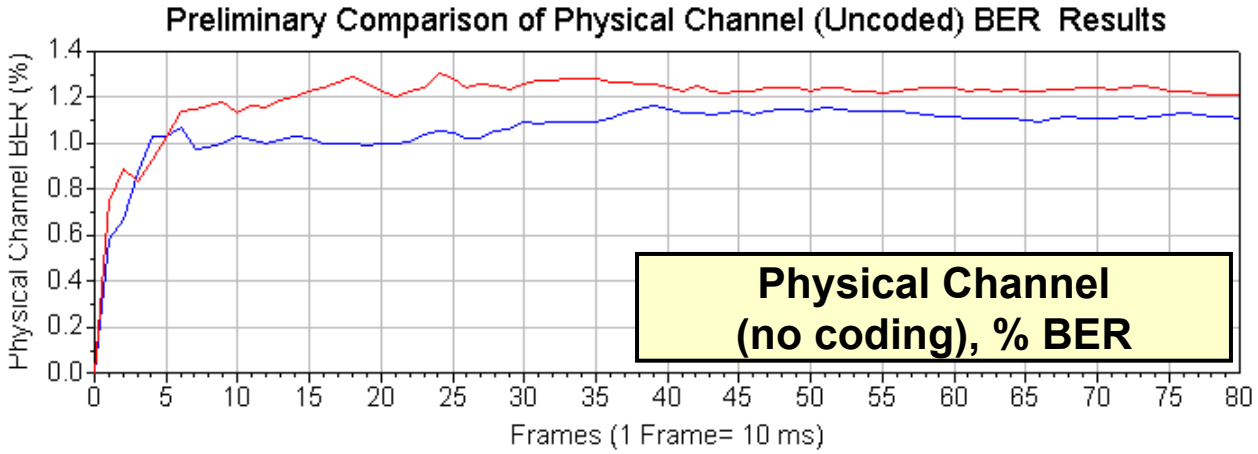
Case Study: Step 6

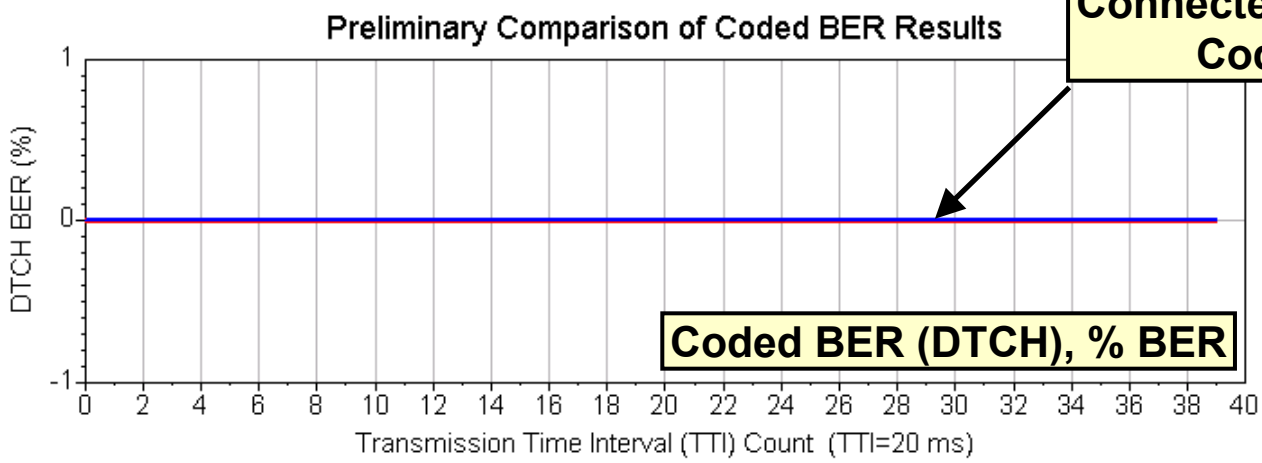
Preliminary Investigation

Compare Connected Solutions BER Results to Simulation-Only BER Results (Preliminary Findings)



Blue Trace=
Simulation-Only Results

Red Trace=
Preliminary Connected Solutions Results Using Real HW Source



Connected Solutions and Simulation Coded BER are Both 0 %

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Summary

- ADS can help verify system, RF, and baseband designs together in one simulation design environment
- Agilent ADS Connected Solutions can help in transitioning between design and test for verification throughout the design cycle
- ADS Connected Signal Source and Signal Analysis can help minimize risk throughout the design cycle and reduce development time